II. Independent Claim 1 Is Patentable over the Applied Art

A. Introduction

Independent Claim 1 recites a semiconductor structure with first and second semiconductor regions and a titanium layer having a line width no greater than 0.3 μm. Claim 1 also recites a relationship between the thickness of the second semiconductor region and the titanium layer, such that when the titanium layer is reacted with the second semiconductor region to form titanium disilicide, the titanium disilicide is in ohmic contact with the first semiconductor region and anneals to a phase with a sheet resistance less than 3 ohms/square. Because the applied references, alone or in combination, do not teach each and every one of these elements, Applicants respectfully request that the rejections of independent Claim 1 and its dependent claims be removed. The deficiencies in the applied art will now be discussed.

B. Hu et al.

In the Office Action, it was asserted that element 218 in Figure 2E of Hu et al. is a titanium layer and, without providing a citation, it was also asserted that the titanium layer has a line width of less than 0.25 microns. Applicants respectfully disagree with this assertion. As stated at paragraph 0026 (page 3), element 218 is a conductor layer of tungsten or ***titanium silicide*** — ***not titanium***. Accordingly, element 218 does not correspond to the layer of titanium recited in Claim 1, nor do the calculated thicknesses in the Office Action, which are based on the tungsten or titanium silicide layer, relate to a thickness of a titanium layer.

Further, there is no teaching in Hu et al. that element 218 has a line width of less than 0.25 microns, as asserted in the Office Action. There are two disclosed embodiments in Hu et al. One embodiment lowers resistivity by forming a diffusion barrier using oxygen or nitrogen in a word line stack to prevent diffusion from a bottom silicon layer to a conductor layer. ***There is no***

disclosure in this embodiment of line widths less than 0.3 μm. In the second embodiment, barrier elements are used to form a low-dose matrix in silicon to modify the grain size in the conductor layer in order to lower resistivity. It is this embodiment — not the first embodiment — that relates to sub-0.3 micon word lines. However, Figure 2 and the sections of Hu et al. relied upon in the Office Action for the teaching of the titanium layer relate to the first embodiment, which does not teach line widths no greater than 0.3 μm. Accordingly, even if element 218 were a titanium layer, which it is not, Hu et al. would still be deficient because there is no teaching that element 218 has a line width no greater than 0.3 μm, as recited in Claim 1.

Additionally, in the embodiment that relates to sub-0.25 micon word lines, there is no teaching of the semiconductor structure recited in Claim 1. Hu et al. provides a low resistivity, sub-0.25 micon word-line titanium disilicide device by using a semiconductor structure that is different from the one recited in Claim 1. Whereas the semiconductor structure in Claim 1 has a specific thickness relationship between the titanium layer and the second semiconductor region, the semiconductor structure used in Hu et al. does not. Instead, the semiconductor structure used in Hu et al. has barrier elements that form a low-dose matrix in silicon to modify the grain size in the conductor layer. Accordingly, Hu et al. teaches a different semiconductor structure than the one recited in Claim 1.

Further, Applicants note that Claim 1 is not a product-by-process claim, reciting titanium disilicide made by a particular process. Rather, Claim 1 recites a semiconductor structure with a specific thickness relationship between the titanium layer and the second semiconductor region. Accordingly, Applicants' argument is not that Claim 1 recites a different process to form titanium disilicide than the one used in Hu et al. Rather, Applicants are asserting that the semiconductor structure disclosed in Hu et al., which has a low-dose matrix in silicon to modify

the grain size in the conductor layer, is different from the semiconductor structure recited in Claim 1. Additionally, the deficiencies in Hu et al. are not cured by combining Hu et al. with the other applied references, as discussed in the following sections.

C. Wilson et al.

In the Office Action, it was asserted that Figure 16 in Wilson et al. shows that a sheet resistance of less than 3 ohms/square can be achieved for a titanium layer thickness of greater than 500 Angstroms. Applicants note, however, that there is no teaching in Wilson et al. that this sheet resistance can be achieved with line widths no greater than 0.30 μm, as recited in Claim 1. As discussed in Applicants' specification, as line width decreases, it becomes more difficult to achieve a sheet resistance of less than 3 ohms/square. Because Wilson et al. does not teach how this fine line effect can be overcome, it cannot be assumed that the results shown in Figure 16 are achieved for line widths no greater than 0.30 μm.

When Wilson et al. in combined with Hu et al., the semiconductor structure disclosed in Hu et al. is used with the thickness disclosed in Wilson et al. to achieve the results shown in Figure 16. As discussed above, the semiconductor structure used in Hu et al. has a low-dose matrix in silicon to modify the grain size in the conductor layer and is different from the semiconductor structure recited in Claim 1. Accordingly, the addition of Wilson et al. does not cure the deficiency in Hu et al.

Additionally, there is no teaching in Wilson et al. that the titanium layer thickness relates to the thickness of the second semiconductor region in the way recited in Claim 1. The Office Action asserted that there was no apparent dependence on the recited thicknesses of the titanium layer and the second semiconductor region. Applicants respectfully disagree. As discussed at pages 6-7 of Applicants' specification, Applicants patterned multiple wafers with many titanium

disilicide wires and measured the sheet resistance on individual 0.25 μm width lines. Through these measurements, Applicants found that the thickness of the second semiconductor region plays an important role in determining completeness of conversion of the titanium disilicide wires from the C49 phase to the C54 phase. The results of these experiments are shown in Figure 5 of Applicants' specification, and these experiments show that the recited thicknesses are important in avoiding the fine line effect in ensuring that the formed $TiSi_2$ is in ohmic contact with the first semiconductor region and anneals to a phase with a sheet resistance less than 3 ohms/square.

D. Nakayama et al.

In the Office Action, it was asserted that Nakayama et al. discloses low sheet resistance associated with uniform titanium silicide for 0.18 and 0.25 μm lines with no fine line effect. However, Nakayama et al., like Hu et al., does not disclose the semiconductor structure recited in Claim 1. Nakayama et al. teaches that the exposed gate poly-Si edge is effective for improving the fine line effect because Si atoms are easily supplied at the gate edge region and that its semiconductor structure comprises SiN sidewall over-etching with high selectivity to SiO_2. This is different from the semiconductor structure recited in Claim 1. Accordingly, Nakayama et al. does not cure the deficiencies noted above in Hu et al.

In the Office Action, it was asserted that Claim 1 contains product-by-process limitations (the formation of titanium disilicide by a specific process) and that a teaching of the product alone (titanium disilicide) is sufficient to render Claim 1 unpatentable. Applicants respectfully disagree. Claim 1 is not a product-by-process claim — it does not recite titanium disilicide nor does it recite a particular process used to form titanium disilicide. Instead, Claim 1 recites a semiconductor structure with first and second semiconductor regions and a layer of titanium,

with a thickness relationship between the titanium layer and the second semiconductor region. Because Claim 1 is not a product-by-process claim, a teaching of titanium disilicide alone is not sufficient to render the claim unpatentable. Only a teaching of the recited semiconductor structure can render Claim 1 unpatentable, and Nakayama et al. alone or in combination with Hu et al. or the other applied references fails to yield the recited semiconductor structure.

E. Spinelli et al.

Figure 2 in Spinelli et al. was relied upon for the teaching of a typical doping range of silicon over gate oxides. There was no assertion in the Office Action that Spinelli et al. discloses the recited semiconductor structure in Claim 1, and Spinelli et al. does not cure the deficiencies noted above in the other applied references.

F. Conclusion

Because the proposed combination fails to teach the specific semiconductor structure recited in independent Claim 1, Applicants respectfully request that the rejections of independent Claim 1 and its dependent claims be removed.

III. Independent Claim 7 Is Patentable over the Applied Art

Independent Claim 7 recites a semiconductor structure comprising a first semiconductor region characterized by a boron dopant concentration greater than $1x10^{20}/cm^3$ and a set of titanium silicide conductors directly overlying the first semiconductor region and in ohmic contact therewith, with each conductor having a width no greater than 0.3 μm and at least 90% of the conductors characterized by a sheet resistance less than 3 ohms/square. Claim 7 was rejected in view of the same proposed combination used to reject Claim 1. Applicants respectfully submit that, like Claim 1, Claim 7 is patentable over the applied references.

In both the embodiment in Hu et al. that relates to low resistivity, fine-line titanium silicide and in Nakayama et al., there is no teaching of a first semiconductor region characterized by a boron dopant concentration greater than $1x10^{20}/cm^3$. Further, in Wilson et al., there is no disclosure of either the recited boron dopant concentration or the recited line width. Finally, there is no disclosure of titanium silicide in Spinelli et al. Accordingly, the proposed combination fails to teach each and every element recited in independent Claim 7, and, as a result, Applicants respectfully request that the rejections of independent Claim 7 and its dependent claim be removed.

IV. The Dependent Claims Are Also Patentable over the Applied Art

The dependent claims recite further elements not shown in the proposed combination and, therefore, provide additional grounds of patentability. For example, dependent Claim 8 depends from Claim 1 or 7 and recites that the semiconductor structure comprises a 3-D memory array. In the Office Action, it was asserted that the first three paragraphs of page 1 of Hu et al. disclose a 3-D memory array. Applicants respectfully disagree. The first three paragraphs of Hu et al. state that semiconductor memory devices are comprised of an array of memory cells and that a word line is formed as a two-layer stack. The term "3-D memory" is not meant to refer to a word line formed as a two-layer stack. Rather, a 3-D memory array is meant to refer to a plurality of memory cells arranged in a plurality of layers stacked vertically above one another in a single chip. To clarify the claim, Applicants have amended Claim 8 to include this definition of a 3-D memory array. Because Hu et al. and the other applied references do not teach a plurality of memory cells arranged in a plurality of layers stacked vertically above one another in a single chip, Applicants respectfully submit that dependent Claim 8 is allowable over the applied art.

V. Conclusion

In view of the foregoing remarks, Applicants submit that this application is in condition for allowance. Reconsideration is respectfully requested. If the Examiner has any questions concerning this Amendment, he is asked to contact the undersigned attorney at (312) 321-4719.

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APPENDIX A

8. (Twice Amended) The semiconductor structure of Claim 1 or 7 wherein the semiconductor structure comprises a 3-D memory array, wherein the 3-D memory array comprises a plurality of memory cells arranged in a plurality of layers stacked vertically above one another in a single chip.